LSI Docket No. 99-398 (1003-0549)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. **99-398 (1003-0549)**

Application of: **Brian A. Day**

Group Art Unit: **2133**

Serial No.: **09/589,930**

Examiner: **J. D. Torres**

Filed: **June 7, 2000**

For: **System and Method for Generating Realtime Errors for Device Testing**

BRIEF ON APPEAL

Hon. Commissioner for Patents

Alexandria, VA 22313

Sir:

This is an appeal under 37 CFR § 1.191 to the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office from the final rejection of claims 1-12 of the above-identified patent application. These claims were indicated as finally rejected in an Office Action mailed May 21, 2003. Notice of Appeal was filed August 12, 2003. Three copies of the present Appeal Brief are filed herewith. The $320.00 fee required under 37 CFR § 1.17(c) for filing an Appeal Brief is authorized to be charged to deposit Account No. 12-2252. Also, please provide any extension of time that may be necessary and charge such and/or any other fees that may be due to deposit Account No. 12-2252, but not to include any payment of issue fees.

(1) REAL PARTY IN INTEREST

LSI Logic Corporation of Milpitas, California is the assignee of this patent application, and the real party in interest.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences related to this patent application (serial no. 09/589,930).

(3) STATUS OF CLAIMS

Claims 1-12 are pending in the application.

Claims 1-12 are rejected.

Each of claims 1-12 is provided in an Appendix attached to this Appeal Brief.

(4) STATUS OF AMENDMENTS

Appellants have filed no amendments subsequent to the final rejection contained in the Office Action mailed May 21, 2003.

(5) SUMMARY OF INVENTION

Appellant's invention is a test circuit (30) and method thereof for inclusion on an integrated circuit supporting real-time data testing. The test circuit (30) is utilized in a data communications environment. Particularly, the test circuit (30) is utilized in a data unit receiver exhibiting transference of a data unit sequence (i.e. a sequence of data units). The test circuitry (30) is included on the substrate of an integrated circuit.

The test circuit (30) includes a data unit identifier (34) and an erroneous data verification parameter generator (38). The data unit identifier (34) identifies a data unit other than a next data unit to be transferred in a data unit sequence. The erroneous data verification parameter generator (38) generates an erroneous data verification parameter corresponding to the data unit identified by the data unit identifier (34). The corresponding erroneous data verification parameter signifying non-verification of data content of the identified data unit.

The method includes identifying a data unit other than a next data unit to be transferred in a data unit sequence (see Block 100 of Fig. 3 and accompanying text on page 12 of the specification). The method also includes generating an erroneous data verification parameter signifying non-verification of data content of the identified data unit (see Block 112 of Fig. 3 and the accompanying text on page 12 of the specification).

The identified data unit or group is later transmitted with the erroneous data verification parameter in real-time (Block 116 of Fig. 3 and accompanying text on page 12 of the specification) following the transmission of other data units

and/or data groups having valid data verification parameters. In this manner, a data receiver may be tested to verify the detection of a data content error in real-time and the execution of the software or firmware for processing an exception may be verified.

(6) ISSUE

Whether, under 35 U.S.C. §102(b), claims 1-12 are anticipated by U.S. Patent 4,561,095 (Khan).

(7) GROUPING OF CLAIMS

The claims do no all stand together. Claims 1-6 form a first separately patentable group for purposes of this appeal. Group I is directed to a test circuit for inclusion on an integrated circuit.

Claims 7-12 form a second separately patentable group for purposes of this appeal. Group II is directed to a method for real-time testing of a data receiver with data transmitted from an integrated circuit.

(8) ARGUMENT(S)

35 U.S.C. § 102(b) Rejection of Claims 1-12

Claims 1-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,561,095 issued to Khan ("Khan"). Appellant submits that Khan does not anticipate claims 1-12 since Khan does not teach each and every limitation of claims 1-12.

It is axiomatic that for a reference to anticipate a claim under §102, a single prior art source must contain all its essential elements (see e.g. Herman v.

anticipation is established only if (1) all of the elements of an invention, as stated in a patent claim (see e.g. Transclean Corp. v. Bridgewood Services, Inc., 290 F.3d 1364, 62 USPQ 2d 1865 (Fed. Cir. 2002)), (2) are identically set forth (see e.g. Getcher v. Davidson, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997)), (3) in a single prior art reference (see e.g. Mehl/Biophile International Corp. v. Milgraum, 192 F.3d 1362, 52 USPQ2d 1303 (Fed. Cir. 1999)). It is shown below that Khan does not teach every limitation of claims 1-6 of Group I or of claims 7-12 of Group II.

I. Group I (Claims 1-6)

Group I consists of independent claim 1 and dependent claims 2-6. Claims 1-6 are directed to a test circuit for inclusion on an integrated circuit.

Discussion re: Patentability of Claim 1

1. Claim 1

Independent claim 1 recites:

> A test circuit for inclusion on an integrated circuit comprising:
> a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and
> an erroneous data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier, said corresponding erroneous data verification parameter signifying non-verification of data content of said identified data unit.

2. Khan Does Not Anticipate Claim 1

a. Khan

Khan teaches an error correcting random access memory system that includes a circuit for generation of a plurality of parity bits from a predetermined

combination of data bits of a data word being stored in a random access memory. The plurality of parity bits is stored in the random access memory along with the data bits. The Khan system generates a check word from the data word and the associated parity bits whose state indicates if any of the bits are in error and proceeds to correct the errors.

The Khan system is also operable to insert an erroneous bit into a data word after the plurality of parity bits are generated and stored for the data word. This allows the Khan system to check operation of the check word circuitry.

b. Khan does not teach identifying a data unit of a data unit sequence wherein the identified data word is not a next data unit of the data unit sequence

The test circuit of independent claim 1 requires a data unit identifier that identifies a data unit (e.g. a data word) of a data unit sequence other than a next data unit to be transferred in the data unit sequence. The test circuit thus tests the veracity of a data unit within a data unit sequence that is being outputted from data communication circuitry other than a next data unit to be transferred in the data unit sequence. Thus, as the data stream (sequence) is being outputted or transferred, the data unit identifier of the subject test circuit identifies one of the data units in the data unit sequence other than a next data unit to be transferred in the data unit sequence. This is the data unit that is tested.

As explained in the specification (see the last paragraph on page 2 of the specification), "Integrated circuits used in data communication may contain test

circuitry that supports the intentional inclusion of erroneous data verification parameters so software or firmware that processes detected data errors at a data receiver may be tested. In this manner, the detection of erroneous data content and the processing that occurs in response to such detection may be confirmed." Moreover, it is indicated in the specification on (see the last paragraph on page 3 of the specification), that "one limitation of the test circuitry defined above [(i.e. the prior art)] arises from the timing of the generation of the error condition. To test a data receiver, the data verification parameter is set to an erroneous value for the next data unit to be transferred. As a consequence, only the first data word or group transmitted after the erroneous data parameter is set may be tested at the data receiver. Such testing does not allow a user to predefine the occurrence of a real-time error condition that occurs after the successful transmission of multiple data words or groups that included valid data verification parameters for verification of each word or group."

Against this background, the above-identified limitation of independent claim 1 allows for the real-time testing of a particular data word or group (unit) particularly in a data communications environment. Most particularly, independent claim 1 provides for testing of a data unit in a data unit sequence (i.e. sequential transfer of data units).

In contrast to the above-noted limitation, Khan teaches a random access memory that stores data words that are selectively output. Khan tests the veracity of a particular data word that is stored in the random access memory. The random access memory is not providing a data unit sequence such as would

be performed in data communications circuitry and as recited in independent claim 1. Rather, Khan merely outputs a data word that is stored in a particular location in the random access memory in response to a read command along with stored parity bits related thereto in order to then create a check word that allows correction of the outputted data word. Khan therefore identifies only an individual data word in a random access memory for correction thereof rather than a data unit, other than a next data unit, in a data unit sequence, as presently recited in independent claim 1.

Therefore, in view of the above, it is clear that although Khan does correct a data word residing in a random access memory, Khan is not directed to identifying a data word in a data sequence, wherein the data word is other than a next data word. Particularly, Khan is not directed to data sequences as are utilized in data communication circuitry.

3. Conclusion

In view of the above, it is clear that Khan does not anticipate claim 1 under 35 U.S.C. § 102. Accordingly, withdrawal of the rejection, reconsideration and allowance of Appellant's claim 1 is hereby respectfully requested.

Discussion re: Patentability of Claims 2-6

1. Discussion

The discussion regarding the patentability of independent claim 1 is relevant to the patentability of claims 2-6, since claims 2-6 depend from and incorporate all of the limitations of independent claim 1. Therefore, since Khan has been shown to not anticipate independent claim 1, claims 2-6, which contain additional limitations not taught by Khan, cannot be anticipated by Khan. As a result, claims 2-6 are allowable for the reasons hereinbefore discussed with regard to claim 1.

2. Conclusion

In view of the above, anticipation under 35 U.S.C. § 102 has not been established with regard to the invention of claims 2-6. Accordingly, withdrawal of the rejection, reconsideration and allowance of Appellant's claims 2-6 is hereby respectfully requested.

Group II (Claims 7-12)

Group II consists of independent claim 7 and dependent claims 8-12. Claims 7-12 are directed to a method of real-time testing of a data receiver.

Discussion re: Patentability of Claim 7

1. Claim 7

Independent claim 7 recites:

> A method for real-time testing of a data receiver with data transmitted from an integrated circuit comprising:
> identifying a data unit other than a next data unit to be transferred in a data sequence; and

generating an erroneous data verification parameter signifying non-verification of data content of said identified data unit.

2. Khan Does Not Anticipate Claim 7

The teachings of Khan are provided above with respect to the arguments regarding the non-anticipation of independent claim 1. These arguments are incorporated herein by reference. In view of these arguments as applied to independent claim 7, it is submitted that Khan does not anticipate independent claim 7. Moreover, the following arguments further show that Khan does not anticipate independent claim 7.

a. Khan does not teach real-time testing of a data receiver

The method of claim 7 is directed to real-time testing of a data receiver. Stated in another manner, the method of claim 7 is directed to testing a data unit of a data sequence, i.e. data units of a data stream. This is not taught in Khan. Kahn teaches static testing of a particular data word that is stored in a random access memory. Such static testing of a particular data word in a random access memory is not real-time testing of a data sequence.

b. Khan does not teach identifying a data unit other than a next data unit in a data unit sequence

It has been shown above that Khan teaches testing individual data words that are stored in a random access memory and not the testing of a data word (unit) in a data unit *sequence*. Since independent claim 7 includes the limitation of identifying a data unit other than a next data unit in a data unit sequence, it is axiomatic that Khan does not teach this limitation.

3. Conclusion

In view of the above, it is clear that Khan does not anticipate claim 7 under 35 U.S.C. § 102. Accordingly, withdrawal of the rejection, reconsideration and allowance of Appellant's claim 7 is hereby respectfully requested.

Discussion re: Patentability of Claims 8-12

1. Discussion

The discussion regarding the patentability of independent claim 7 is relevant to the patentability of claims 8-12, since claims 8-12 depend from and incorporate all of the limitations of independent claim 7. As a result, claims 8-12 are allowable for the reasons hereinbefore discussed with regard to claim 7. Therefore, since independent claim 7 has been shown to not be anticipated by Khan, claims 8-12, which contain additional limitations not taught by Khan (i.e. not anticipated by Khan), cannot be anticipated by Khan.

2. Conclusion

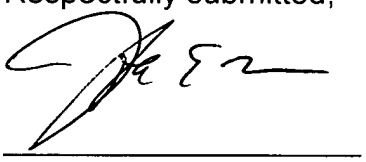
In view of the above, anticipation under 35 U.S.C. § 102 has not been established with regard to the invention of claims 8-12. Accordingly, withdrawal of the rejection, reconsideration and allowance of Appellant's claims 8-12 is hereby respectfully requested.

(9) CONCLUSION

In view of the above, it is respectfully submitted that claims 1-12 are not anticipated under 35 U.S. C. §102(b) by U.S. Patent 4,561,095 issued to Khan.

Thus, the Board of Appeals is respectfully requested to reverse the rejection of these claims.

Respectfully submitted,



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(10) APPENDIX

1. A test circuit for inclusion on an integrated circuit comprising:

a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and

an erroneous data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier, said corresponding erroneous data verification parameter signifying non-verification of data content of said identified data unit.

2. The test circuit of claim 1, wherein said erroneous data verification parameter generator inverts a data verification parameter generated from said data content of said selected data unit.

3. The test circuit of claim 1, wherein said erroneous data verification parameter generator inverts a portion of said data content of said selected data unit that is used to generate a data verification parameter.

4. The test circuit of claim 1, wherein said data unit identifier identifies a data group and said erroneous data verification parameter corresponds to said identified data group.

5. The test circuit of claim 1, wherein said data unit identifier uses data unit content to identify said data unit.

6. The test circuit of claim 1, wherein said data unit identifier uses data unit position to identify said data unit.

7. A method for real-time testing of a data receiver with data transmitted from an integrated circuit comprising:

identifying a data unit other than a next data unit to be transferred in a data sequence; and

generating an erroneous data verification parameter signifying non-verification of data content of said identified data unit.

8. The method of claim 7, wherein said generation of said erroneous data verification parameter includes inversion of a data verification parameter generated from said data content of said selected data unit.

9. The method of claim 7, wherein said generation of said erroneous data verification parameter includes inversion of a portion of said data content of said selected data unit that is used to generate a data verification parameter.

10. The method of claim 7, wherein said identification identifies a data group and said generated erroneous data verification parameter corresponds to said identified data group.

11. The method of claim 7, wherein said identification identifies a data unit using data unit content of said data unit.

12. The method of claim 7, wherein said identification identifies a data unit using position of said data unit in a data sequence.